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09/880,090	06/14/2001	Yasunori Satoh	OKI 276	3818

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EXAMINER	
NATNAEL, PAULOS M	
ART UNIT	**PAPER NUMBER**
2614	7

DATE MAILED: 04/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/880,090	Applicant(s) SATOH, YASUNORI	
	Examiner Paulos M. Natnael	Art Unit 2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-7 and 10-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-7 and 10-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. As indicated in the previous Office Action Summary, Priority to Japanese application number 191731/1999 has been claimed by Applicant, however, no certified copies have been received so far.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims **1,2,4-7,10-13** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim **1** (as amended), the claimed "calculated difference signal" output from the judgment circuit does not appear to be utilized anywhere, and, the selector combines the plurality of delayed input data but does not appear to output any signal to anywhere, rendering the claim indefinite.

In claim **6** (as amended), the claimed calculated "difference signal" and "delayed signal" both of which output by the judgment circuit do not appear to be utilized anywhere in the system, again rendering the claim indefinite;

In claim **7** (as amended), the delayed signal output from the judgment circuit does not appear to output any signal, rendering the claim indefinite.

Claims **2,4,5, 10-13** are rejected for being dependent of the rejected claims as shown above.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims **1,2,4 and 5** are again rejected under 35 U.S.C. 103(a) as being unpatentable over Hickman, U.S. Pat. No. **5,694,432** in view Wang, U.S. Pat. No. **5,796,796.**

Considering claim **1**, Hickman discloses the following claimed subject matter, note;

b) a counter circuit that counts a pixel number of each line in the input data, is met by t FIFO count 48, Fig.4;

c) a judgment circuit that calculates a difference between the standard number and the pixel number counted by the counter circuit, and outputs a calculated difference signal, is met by the Control circuit 53 and multiplexer 44, fig.4.

Except for;

a) a delay circuit delaying the input data with a plurality of delay times so that the delay circuit outputs a plurality of delayed input data;

Regarding a), Hickman discloses a Dual Port FIFO 42. Hickman teaches that as another modification, the continuous input series of data bits S.sub.i which occurs on input terminal 10a of the transmitter 10 consists of pixels in successive video frames. These pixels are generated by a camera 160, a sample and hold circuit 161, and an analog-to-digital converter 162 which are serially intercoupled to each other as shown in FIG. 13. (col. 21, lines 10-16) Hickman does not specifically disclose delay circuit that output as plural output signals. Using multiple delay elements and selecting circuits to select the multiple inputs/outputs from the delay elements, however, is well known in the art.

In that regard, Wang discloses a pointer adjustment jitter cancellation processor utilizing phase hopping and phase leaking techniques. Fig.3 of Wang discloses the phase hopping controller comprising an array of delay elements 180, an address generator/counter 160, and a multiplexer 170 that selects among the multiple outputs of the delay elements. (col. 5, lines 48-57)

Therefore, it would have been obvious to the skilled in the art at the time the invention was made to modify the reference of Hickman by providing the controller 150 of Wang in order for the system to be able to select from the multiple delayed output signals.

Considering claim **2**, wherein the delay circuit includes a plurality of flip-flop circuits, converting the input data into the delayed input data with each delayed by one clock,

See rejection of claim 1(a);

Considering claim **4**, a video signal control circuit as claimed in Claim 1, wherein the judgment circuit is able to set an initial value of the delay to the delay circuit in accordance with a selection signal, is met by the DB count 51 and ZD 52, fig.4;

Considering claim **5**, a video signal control circuit as claimed in Claim 4, further comprising an initial value judgment circuit that judges an inclination of a pixel dispersion on the basis of the pixel number counted by the counter circuit, and outputs the selection signal that designates an initial delay in accordance with the inclination of the pixel dispersion.

See rejection of claim 4.

Response to Arguments

6. Applicant's arguments filed Jan 26, 2004 have been fully considered but they are not persuasive.

Applicant's Arguments

a) Hickman provides no suggestion that the pixels or video signal would be treated any differently that the more general data input discussed earlier.

b) Wang is directed to a pointer adjustment jitter cancellation processor. Wang does disclose a plurality of delay circuits as pointed out by the Examiner. However, in Wang, the delay circuits delay a compensated write clock signal rather than "delaying the input data with a plurality of delay times so that the delay circuit outputs a plurality of delayed input data" as amended claim 1 requires. It is clear that the combination suggested by the Examiner is not suggested by the references considered as a whole, and even if it were, the combination of Hickman and Wang would not yield the claimed invention.

Examiner's response

a) The claims as recited or as amended do not recite that the pixels or video signal would be treated nay differently than the more general data input, either. Thus, the applicant is arguing something that is not found in the claims.

b) the delay circuits of Wang in fig. 3 delay the input data for different times; i.e, the output from each delay device is delay by some desired time. Thus, Wang still meets the claimed language as recited. As to the combination, delay circuits are well known in the art and it would have been obvious to the skilled in the art at the time the invention was made to modify the system of Hickman by providing a delay circuit that generates a plurality of delayed signals at the output.

Allowable Subject Matter

7. Claims **6 and 7** would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action.

8. Claims **10-13** would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Urbansky et al, U.S. Pat. No. 5,359,605 discloses a circuit arrangement for adjusting the bit rates of two signals, wherein the selecting matrix 5 is disclosed to include a plurality of delay elements V1-V7 and selecting circuits A1-A8.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paulos M. Natnael whose telephone number is (703) 305-0019. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Miller can be reached on (703) 305-4795. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PMN
April 2, 2004

PAULOS M. NATNAEL
PATENT EXAMINER